BRINGING RF TUNABILITY TO MOBILE COMMUNICATIONS MARKETS

Peter Bacon (Peregrine Semiconductor, Nashua, NH, USA; pbacon@psemi.com)

ABSTRACT

Peregrine Semiconductor's UltraCMOS™ technology has demonstrated superior RF performance in comparison to other Silicon and SOI based processes. Utilizing this advanced silicon-on-sapphire technology provides an unprecedented level of RF performance while supporting high levels of analog and digital integration that bulk CMOS is known for. This paper will discuss fundamental RF tuning techniques made possible with UltraCMOS that support antenna impedance and frequency tuning, power amplifier multi-mode operation, and power control implementations.

1. INTRODUCTION

The ongoing proliferation of frequency bands and channel access schemes required by Smartphones and the civilian cellular network are forcing hardware suppliers to rethink the architecture of the RF Front End. The emerging trend is away from fixed RF channels for each access scheme and frequency band towards a more tunable and reconfigurable architecture. Functional reuse is on the rise and frequency tuning is beginning to have a presence in the handset market.

Peregrine Semiconductor is pursuing several developments necessary for the next generation reconfigurable RF Front End, including antenna frequency band tuning and impedance matching. Multi-mode operation of power amplifiers has been demonstrated and is a critical building block to future generation front ends. Finally, in support of the ever increasing complexity of the front end, the ability to integrate sensing and control circuitry in a low cost, integrated fashion provides tremendous leverage and capability for implementing complex control algorithms.

Peregrine's UltraCMOS Silicon-on-Sapphire (SOS) technology enables a high performance RF device on an ideal, insulating substrate coupled with analog and digital integration levels for which bulk CMOS processes are known. The strength of this unique combination of RF performance with analog and digital integration has already proven itself in matters of cost, volume, and reliability/quality for the cellular market. Utilizing the potential of UltraCMOS processing in areas of RF tunability and multi-mode reconfiguration is a natural extension of this technology.

2. RF FRONT END

A common architecture used in today's Smartphones is shown in Figure 1. The architecture uses individual power amplifiers to address the GSM 2G and WCDMA 3G transmit requirements. As can be seen in the basic architecture, little functional reuse exists and each transmit arm is uniquely defined by access scheme and frequency band. A few points of functional reuse do currently exist in the GSM paths and at the antenna. The two individual transmit paths supporting GSM cover two distinct frequency sub-bands within each path: 824-849MHz and 880-915MHz, 1710-1785MHz and 1850-1910MHz. Commonly, this multi-band coverage is simply part of the amplifier's bandwidth design requirement and no frequency tuning is used in the amplifier or subsequent low pass filtering to achieve this coverage. Historically designers believed that the incremental improvement achieved by narrowband tuning for the sub-band frequencies was counter balanced by the increased product cost and signal loss that come with it.

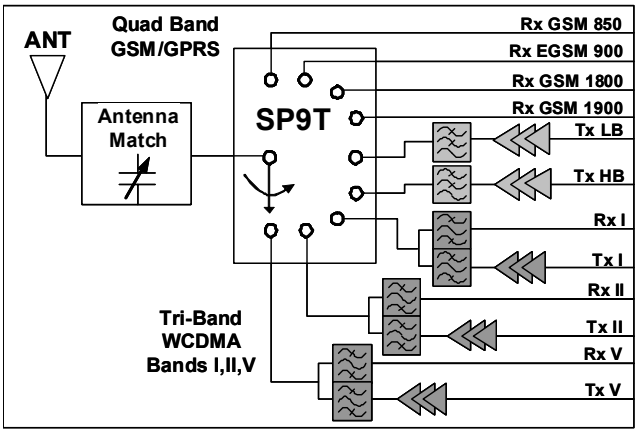

Figure 1 Today's Smartphone RF Front End Architecture

In contrast to simply broad banding an amplifier's frequency response across a 10-15% bandwidth, frequency tuning is beginning to be utilized at the RF antenna. Narrowband frequency tuning can improve the antenna efficiency and minimize antenna coupling with surrounding circuitry [1]. This design is being implemented so that a single antenna element can be used across broadly spaced

frequency bands and for optimum tuning over the 3-4% bandwidth of the sub-bands. Switched capacitors and switched antenna structures can be used to provide the frequency tuning, resulting in a reduction in total system loss and a boost in battery life.

In addition to frequency tuning (the setting for which is easily determined by access scheme, world location, and service provider), antenna impedance matching is a tuning concept that requires real time parametric measurement of incident and reflected power levels and modifying the tuning network accordingly. Antenna impedance matching is employed to minimize the output power of the user equipment's power amplifier while maintaining the required link budget to support an acceptable BER. Stated differently, the tuning process attempts to minimize the total loss between the power amplifier's output and the base station receiver thereby maximizing the total radiated power (TRP) of the handset. The net result of the tuning is that the user's power amplifier operates at a power level 0-4dB less than if the antenna impedance were not tuned. The real time antenna impedance tuning attempts to counteract the negative pulling effects caused by the user's hand, head, and other items that maybe in close proximity to the antenna, such as tables, car interiors, etc. This real time adjustment to TRP translates to better cell coverage and improved battery life. Recall that 3dB less power is a factor of 2 reduction in output power.

Apart from applications at the antenna, reconfiguration tuning, and functional re-use are not widely used in today's cellular handset RF Front End. Increased costs, loss in performance, and reliability issues have often out weighed the system flexibility that is achieved by implementing a more frequency and mode agile RF Front End. To counter these issues, Peregrine Semiconductor has been focused on providing solutions to the RF Front End that keep these key commercialization metrics as foundational.

3. MULTI-MODE POWER AMPLIFIER

Multi-mode power amplifier operation commonly implies supporting multiple access schemes while maintaining state of the art power added efficiency (PAE) performance in each of the operational modes. Common in today's handsets are multi-mode GSM/GPRS/EDGE power amplifiers that can operate in both a constant envelope, saturated mode (GSM & GPRS) and in a non-constant envelope, linear scheme (EDGE). The frequency and time slot compatibility between GSM, GPRS and EDGE helps facilitate the reuse of a single PA chain for all three schemes. This multi-mode implementation is often achieved through simple bias adjustments and power control changes in the PA. Little if any RF tuning is required to operate in both the linear and saturated modes.

The next generation handset envisions the multi-mode power amplifier expanding to include both a shift in frequency and the addition of the WCDMA HPSK and LTE QAM modulation schemes. Both of these constraints put additional pressure on the power amplifier. The push to 3G and 4G is driven by the ever growing need to support more wireless data transmission. The increase in data rates from 2G to 4G is impressive, but the technical challenge to maintain PA efficiency and handset talk/transmit time also increases.

Today there are products at the module component level that support multi-mode operation relying upon switch matrices to switch between distinct amplifiers, one for 2G and one for 3G. Figure 2 shows one such architecture.

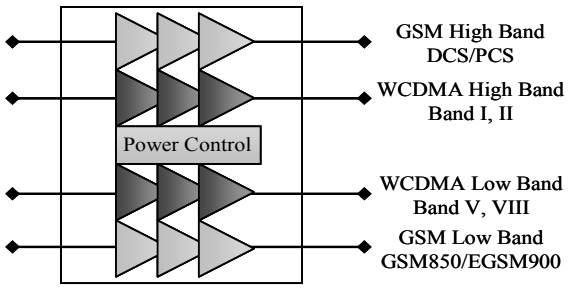

Figure 2 Multi-Mode Multi-Band PA Module Architecture

The move to a truly converged multi-mode PA requires the fundamental technology and device performance to be able to support the two modes of operation with competitive performance in both modes. A compromise in peak power efficiency is not easily accepted by the market place, and regardless of any gains that maybe achieved over the phone's entire operational probability density function (PDF), peak PAE is still a recognized competitive metric. Figure 3 depicts the performance that Peregrine has achieved for a common output device comparing three different operational regimes: WCDMA, EDGE, and GMSK.

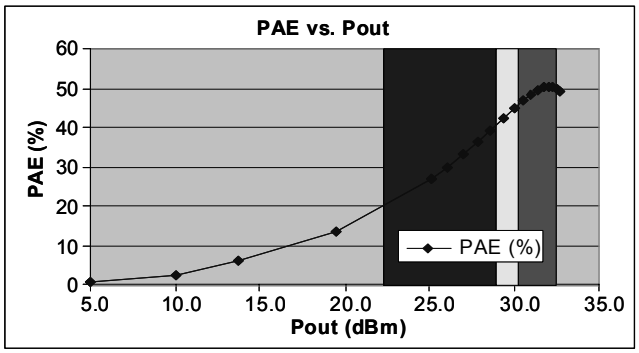

Figure 3 UltraCMOS PA Power Added Efficiency

At the heart of 3G multi-mode operation is the need to reconfigure the power amplifier to operate in different classes of operation. For WCDMA/linear and GSM/saturated, the two most common classes are, respectively, Class AB and Class E. The primary difference between these two modes can be described by their dynamic load line. Under Class AB at full power the signal transverses a load line ideally depicted by a straight line of constant slope over the I-V plane. Juxtaposed to this behavior, the Class E amplifier attempts to transverse a path that follows the I (V=0) and V (I=0) axes with its output signal in order to approach the theoretical peak efficiency of 100%. Peak PAEs achieved in today's wireless handset power amplifiers are greater than 40% and 50% respectively for Band I WCDMA and DCS/PCS GSM.

With the move in 4G to more complex modulation schemes such as 64 QAM comes the need for greater transmission accuracy. This, in turn, requires that the transmission path be extremely linear. There are known techniques at the device level that help improve the power amplifier's linearity performance [2][3] but these techniques have limited benefit in reducing the margin that the power amplifier needs to have to support higher peak-to-average (PAR) ratios of the more complex schemes. Alternatively, predistortion techniques, both analog and digital, can be employed to drive the amplifier even harder towards peak saturated power. These techniques are commonly employed in today's base station amplifiers to achieve unprecedented PAEs. Their use in handset applications is less straightforward due to the increased sensitivity to cost and because the transmitted output powers are orders of magnitude lower. So, although demonstrated to provide improved PAE and peak output power for a given device, the incremental cost and signal processing power consumption tend to out weigh the benefits achieved. Figure 4 shows the performance measured for an UltraCMOS-based PA under WCDMA modulation with and without predistortion.

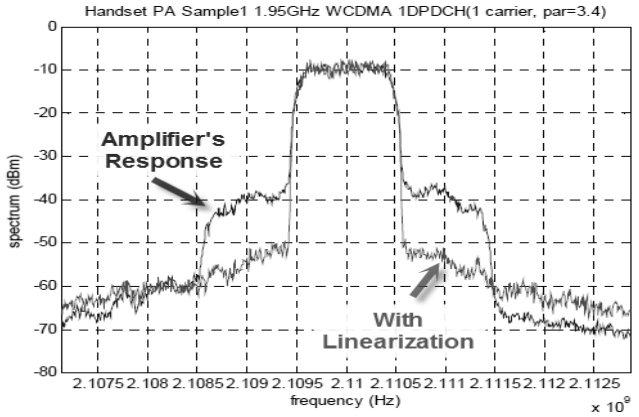

Figure 4 UltraCMOS WCDMA PA ACLR Performance

The strength of UltraCMOS technology lies in its ability to integrate these concepts in support of multi-mode and optimum performance in a single integrated IC.

4. DIGITALLY TUNABLE CAPACITOR

In order to incorporate RF tuning to realize different impedances or to move to other center frequencies one needs to have the ability to change reactance values. And if narrow band performance is to be maximized and the loss minimized, the unloaded quality factor of the tuning mechanism Q_u, defined as energy stored versus energy lost, must be maximized.

Achieving a tunable reactive element with a high Q_u – while being linear, able to handle high power levels of more than one watt, and that can be integrated anywhere where a variable reactance is needed – is a daunting challenge. Some options exist and have demonstrated various levels of performance [4], [5], but often fall short on the integration path requiring either multiple technologies to form a solution or additional processing steps to the fundamental technology that may compromise reliability and yield.

To address this market need, Peregrine engineers developed DuNE™ technology, a design methodology which uses the building blocks of UltraCMOS processing. DuNE design techniques have enabled a digitally tunable capacitor (DTC) (Figure 5).

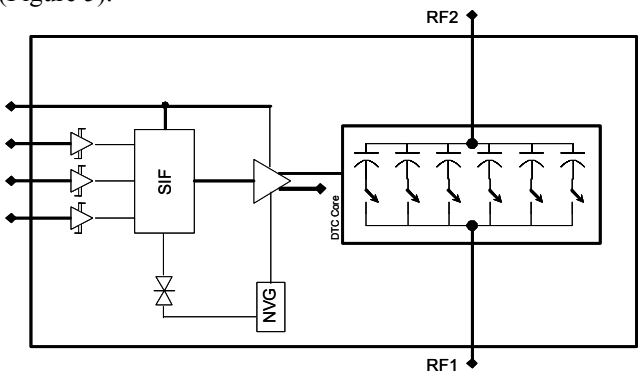

Figure 5 DTC Functional Block Diagram and Simplified Schematic

The digitally tunable capacitor (DTC) relies upon a high Q capacitor bank at its core to provide the required capacitor tuning range. Since the maximum capacitance is defined by the total capacitor area and the minimum capacitance value by the bit structure and number of bits, there is virtually no tuning range limit imposed by the fundamental capacitor technology. Monotonic tuning ranges in excess of 10:1 have been demonstrated while still meeting power and linearity constraints common to cellular handsets. Removing the constraint of linear or geometric weighted capacitance

structure, discrete switched capacitor values required for specific frequency tuning or modes of operation are also possible. And a mix of large discrete capacitance steps combined with small, fine tuning capacitance steps can provide major band tuning with the ability to absorb manufacturing tolerances through calibration or real time feedback via control loops.

Typical DTC performance is shown in the following figures. Figure 6 shows the tuning range for a DTC targeting the Mobile TV handset market. The capacitance range is defined in Figure 6 while Figure 7 shows the unloaded Q versus frequency for several states. Figure 8 is a die photograph of the DTC as configured for a single DTC.

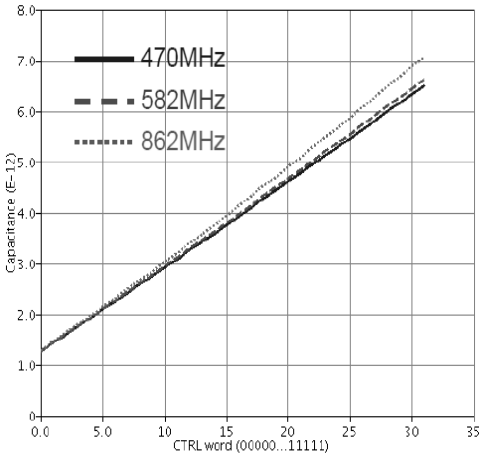

Figure 6 DTC Capacitance Tuning Range for Mobile TV

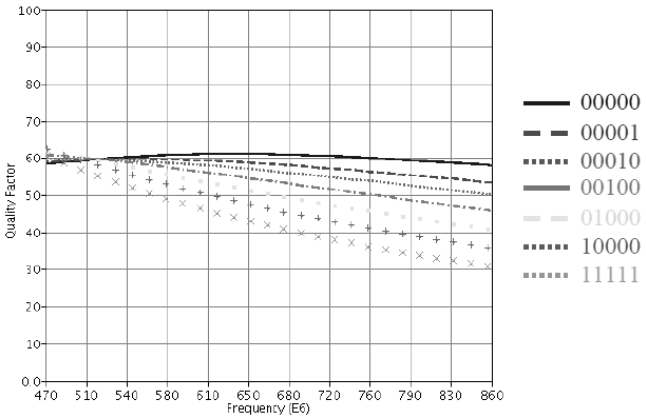

Figure 7 Unloaded Q vs. Frequency for Multiple States

The flexibility to scale the DTC architecture for power is another significant attribute. The dominant constraint for power handling is the switch device that is used to connect in different capacitance values. By modifying the device stack height used for the DTC, the required power, voltage, and current levels can be readily designed for. The DC isolation achievable in silicon-on-sapphire permits stacking several devices while maintaining ideal voltage division across the entire stack and incurring no leakage to the substrate. The net result of this is a very flexible, tunable reactance that can be placed anywhere within the circuit requiring tuning, and the device optimized to fit the capacitance range and power requirements. Figure 9 shows a DTC used in a feedback loop around a large power device. In this case the four different feedback settings can be selected to alter the R-C feedback to affect the effective input impedance. The figure shows both the top and bottom side of the circuitry for clarity.

One last attribute of the DTC is its digital interface. Stand-alone DTC products from Peregrine use common two- and three-wire interfaces such as I^2C, SPI, and MIPI. At the fundamental RF core, single control lines are used to switch the capacitance value of each segment. This level of control and interface is readily accomplished with the inherently CMOS silicon-on-sapphire UltraCMOS process. A full complimentary CMOS digital library speeds implementing digital logic and algorithmic control circuitry.

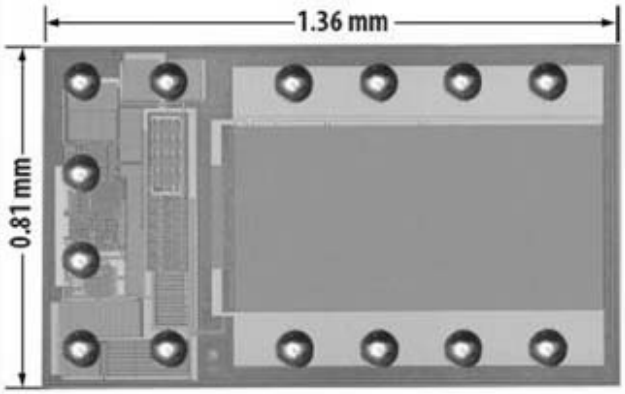

Figure 8 DTC Die Photograph: Die Area = $1.1mm^2$

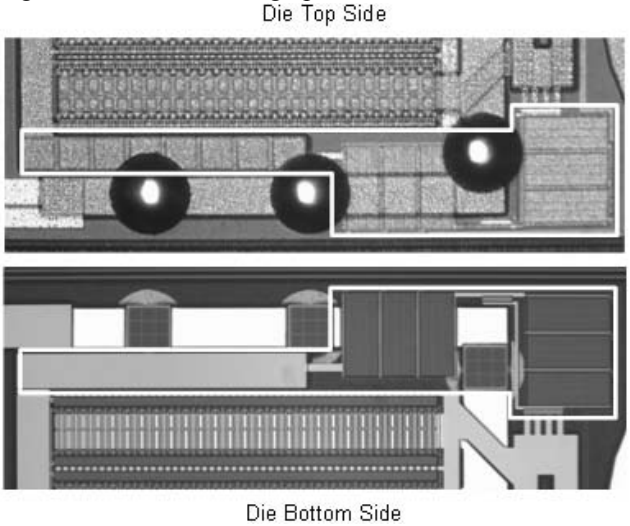

Figure 9 DTC Integrated as Part of a Feedback Loop

5. INTEGRATED POWER CONTROL

A key aspect of any handheld wireless device is maximizing battery life, and a major factor affecting battery life is the transmit power requirement. In all of today's cellular networks, power control is implemented so that only the bare minimum output power is used to support the required link budget. The network determines with what power level the handset should transmit and the handset, in concert with the specific power amplifier architecture and features, determines how best to address the specific transmit power level. At the RF power amplifier level various methods have been employed to achieve variable output power. The two fundamental approaches can be classified as varying and non-varying load line. Figure 10 describes the basic difference. In the case of varying load lines, either the current or voltage is changed and the dynamic load line is varied. In the case of non-varying both current and voltage are reduced to maintain a constant slope in the I-V trajectory.

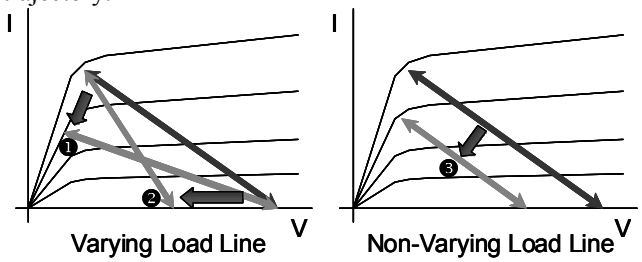

Figure 10 Varying and Non-Varying Load Line Power Control: 1-Reduced Current, 2-Reduced Voltage (rarely employed alone), 3-Constant Slope

At peak power, the power amplifier is optimized at the nominal battery voltage to give optimum efficiency while also maintaining the RF performance of the channel, usually specified in terms of a non-linear metric such as error vector magnitude (EVM). This is a multi-faceted trade-off that varies device periphery, bias operating conditions, and impedance matching to achieve optimum performance for a given technology.

Common techniques for optimizing the efficiency at backed off power levels have been summarized elsewhere [8]. Peregrine Semiconductor has demonstrated several of these techniques in its own power amplifier and power management development. Two of these techniques will be explored in more detail: drain voltage power control (for use in maintaining a non-varying load line) and drain current power control.

At the heart of the drain voltage power control scheme is a buck DC-DC converter. The goal of the DC-DC converter is to efficiently convert the nominal battery voltage down to a lower voltage so that the backed off power added efficiency is improved. Figure 11 shows a common block diagram. The benefits of UltraCMOS' lossless sapphire substrate are leveraged to reduce device parasitics, which in turn leads to faster, lower loss switching of the core DC-DC circuit. The faster clock speed of the DC-DC converter permits placing the clocking frequency above 20MHz and outside the bandwidth of the modulation easing the handling of any DC-DC spurious and permitting a smaller footprint for the filtering/isolation inductor.

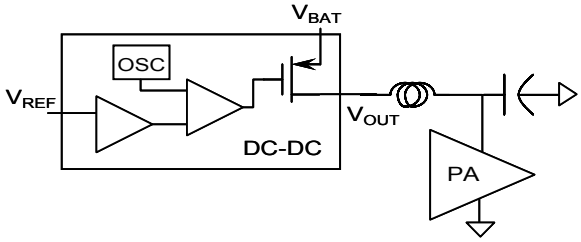

Figure 11 Drain Voltage Power Control Block Diagram

Drain current power control is implemented by modifying the bias conditions of the power amplifying devices. This can be set to predetermined voltage or current levels using common CMOS voltage references and current mirroring techniques. Figure 12 depicts the block diagram of a bias control circuit that takes into account the battery voltage, the current density targeted, and the manufacturing variances to provide three distinct bias voltages VG1, VG2, and VG3.

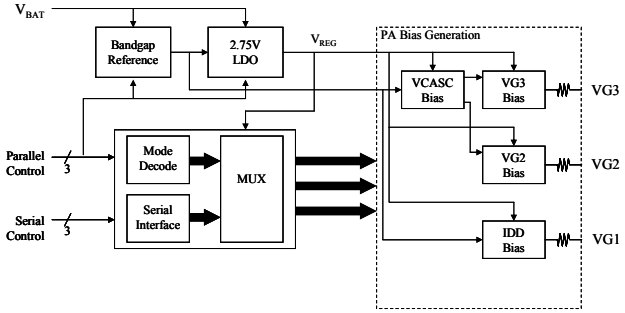

Figure 12 Drain Current Power Control block diagram

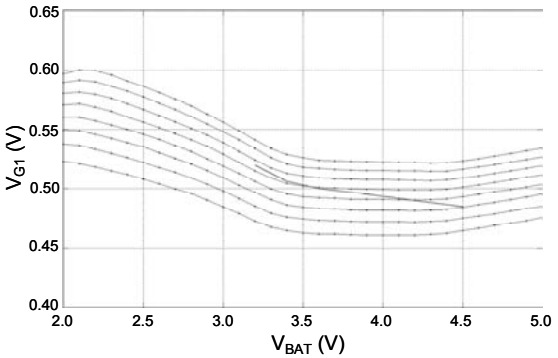

Figure 13 Depicts the Primary Bias Voltage, VG1 as a Function of Battery Voltage and Current Setting (the reference line denotes nominal design target)

Although these integrated forms of tuning are bias voltage and current related, these techniques are designed to optimize the RF performance across a broad range of transmit power and they go hand-in-hand with other RF tuning techniques to assure optimum RF performance.

6. INTEGRATION

Integration of the tuning capabilities discussed above is a key strength of UltraCMOS technology. The ability to monitor and adjust the RF channel through integrated sensing and detection simplifies the signal routing and minimizes the perturbation of the system. Optimizing the tuning mechanism size and impact based upon the requirements, such as tuning range and power handling, and not solely upon technology constraints is a tremendous advantage that can be leveraged throughout the integrated circuit.

Figure 14 shows an integrated GSM/GPRS power amplifier with integrated SP6T switch. The power amplifier has integrated drivers along with an on-chip pass device for implementing power control. All aspects of the chip are optimized for the peak GSM power levels and isolation requirements. A critical isolation requirement, Tx to Rx isolation, is better than 45dB and 35dB for Low Band and High Band respectively. Amplifier Pout is 35dBm and 32dBm and switch insertion loss < 0.6dB and 1.0dB for transmit for low band and high band.

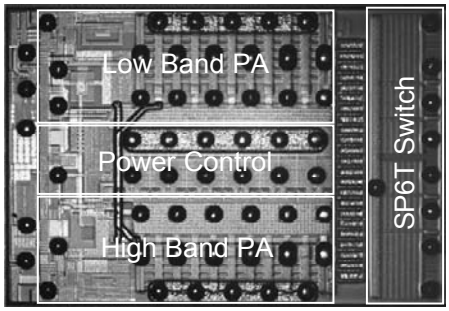

Figure 14 GSM/GPRS Power Amplifier & SP6T Switch

Antenna impedance matching requires monitoring the incident and reflected waves at the antenna interface. Integration of the couples and power detectors, control loop state machine, and digital control interface, and stable reference voltages are all possible using the UltraCMOS technology. Coupler loss can be kept below 0.25dB, and power detection can be achieved with less than 0.1dB of insertion loss being added. In total, a full impedance tuner can be implemented with less than 1.2dB of total loss at a nominal 50 ohm setting in the cellular frequency bands. This nominal loss is readily justified when the capability of the tuner is engaged to transform an 10:1 VSWR, 4.8dB mis-match loss into a <2:1 VSWR with less than 0.5dB mis-match loss. Figure 15 represents a dual band DTC 2x2 matrix that is the tuning core of a complete low band /high band antenna impedance tuner module.

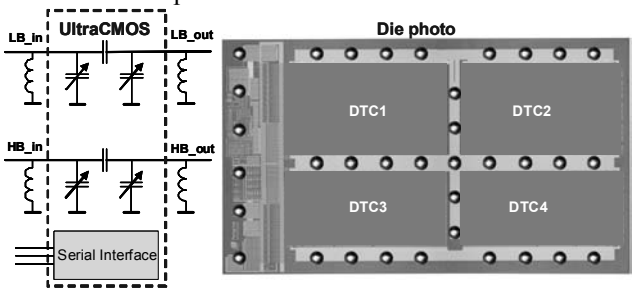

Figure 15 Antenna Impedance Tuner

7. CONCLUSION

The ability to integrate high performance RF circuitry with analog and digital functions provides the foundation for RF tunability. The requirement to support tunability at wireless power levels in the 1 Watt range requires high linearity and power handling capability that bulk CMOS, and even SOI, can not support as effectively as Silicon on Sapphire. Peregrine's UltraCMOS technology provides an optimum RF substrate that lets the native CMOS devices perform without the hindrances of substrate parasitics. This, in turn, supports the linearity and power requirements historically delegated to Gallium Arsenide and other more exotic III-V compound semiconductors.

In this review several aspects of tunability were discussed that have been developed and demonstrated by Peregrine Semiconductor. This summary represents the combined work of multiple teams and individuals within Peregrine. Work continues towards a more integrated, multi-mode and multi-band RF channel that includes reconfigurable filtering.

8. REFERENCES

[1] J Shamblin, "Is 2 dB Worth $2", Antenna Systems and Technology Conference, Austin, TX, Sep 2008 (http://www.ethertronics.com/file_library/AST Ethertronics Is 2dB Worth $2_FINAL.pdf)

[2] J. Martins, et. al, "A Metric for the Quantification of Memory Effects in Power Amplifiers", IEEE Transactions on Microwave Theory & Techniques, Vol 54, No. 12, Dec 2006, p4432- 4439.

[3] M. Zhao, "A 2.45GHz CMOS Power Amplifier with High Linearity", International Conference on ASIC, ASICON 2009, Oct 2009, p383-386

[4] R. C. Johnson, "RF-MEMS aims to tune mobile wireless", EE Times, Nov 12, 2007

[5] "Paratek is Shipping High Performance AIMM Evaluation Kits", Microwave Journal, June 2008.